



SMC-00-299C

October 22, 2003

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/623,907 07/18/03 |
| Chao-Chieh Tsai et al. |
| HIGH fmax DEEP SUBMICRON MOSFET |
| Grp. Art Unit: |
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INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on October 23, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 10/23/03

U.S. Patent 5,731,239 to Wong et al., "Method of Making Self-Aligned Silicide Narrow Gate Electrodes for Field Effect Transistors Having Low Sheet Resistance," describes a method of fabricating self-aligned silicide narrow gate electrodes for field effect transistors (FET) having low sheet resistance.

U.S. Patent 5,268,330 to Givens et al., "Process for Improving Sheet Resistance of an Integrated Circuit Device Gate," describes a process for improving sheet resistance of an integrated circuit device gate.

U.S. Patent 5,554,544 to Hsu, "Field Edge Manufacture of a T-Gate LDD Pocket Device," describes a field edge method of manufacturing a T-gate LDD pocket device.

U.S. Patent 5,739,066 to Pan, "Semiconductor Processing Methods of Forming a Conductive Gate and Line," describes a semiconductor processing method of forming a conductive gate or gate line over a substrate.

U.S. Patent 6,063,675 to Rodder, "Method of Forming a MOSFET Using a Disposable Gate with a Sidewall Dielectric," describes a method of forming a MOSFET using a disposable gate with a sidewall dielectric.

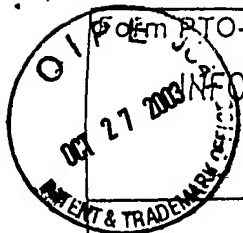
TSMC-00-299C

U.S. Patent 5,943,560 to Chang et al., "Method to Fabricate the Thin Film Transistor," describes a method of fabricating a thin film transistor using ultrahigh vacuum chemical vapor deposition (UHV/CVD) and chemical mechanical polishing (CMP) systems.

Sincerely,

A handwritten signature in black ink, appearing to be 'SBA', written over the word 'Sincerely,'.

Stephen B. Ackerman, Reg. #37761



1 of 1

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| Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION (Use several sheets if necessary) | Doc No. Number (Sequence) | Application Number |
| | TSMC-00-299C | 10/623,907 |
| | Applicant Chao-Chieh Tsai et al. | |
| | Filing Date 07/18/03 | Drawn Art Unit |

U. S. PATENT DOCUMENTS

| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | NUMO DATE & APPROPRIATE |
|---------------------|-----------------|---------|---------------|-------|----------|----------------------------|
| | 5731239 | 3/24/98 | Wong et al. | 438 | 296 | 1/22/97 |
| | 5943560 | 8/24/99 | Chang et al. | 438 | 151 | 4/19/96 |
| | 6063675 | 5/16/00 | Rodder | 438 | 291 | 10/24/97 |
| | 5739066 | 4/14/98 | Pan | 438 | 595 | 9/17/96 |
| | 5554544 | 9/10/96 | Hsu | 437 | 35 | 8/9/95 |
| | 5268330 | 12/7/93 | Givens et al. | 437 | 195 | 12/11/92 |
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FOREIGN PATENT DOCUMENTS

| DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | Translation | |
|-----------------|------|---------|-------|----------|-------------|----|
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OTHER DOCUMENTS (Including Author, Title, Date, Portinart Pages, Etc.)

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| EXAMINER | DATE CONSIDERED |
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant